Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated circuit comprising an array of DRAM cells, each DRAM cell comprising:

a first transistor having a gate coupled to a read word line and a drain coupled to a read bit line;

a second transistor coupled in series between the first transistor and a power supply voltage; ~~and~~

a third transistor coupled between the gate of the second transistor and a write bit line, a gate of the third transistor being coupled to a write word line; [[,]]

a capacitor coupled to a gate of the second transistor; and

a pass gate coupled to the gate of the second transistor and the capacitor,

wherein the write word line is not directly connected to the read word line, and

wherein a voltage stored on the capacitor directly drives a gate voltage of the pass gate.

2. (Currently Amended) The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array, and the gate of the second transistor is coupled to [[a]] the pass gate in the field programmable gate array.

3. (Currently Amended) The integrated circuit according to claim [[2]] 1 wherein the pass gate is a programmable routing connector that couples interconnect lines on the field programmable gate array.

4. (Currently Amended) The integrated circuit according to claim [[2]] 1 wherein the pass gate is used to configure logic performed by logic circuitry on the field programmable gate array.

Claim 5. (Canceled)

6. (Currently Amended) The integrated circuit according to claim [[5]] 1 wherein the capacitor is a planar capacitor or a trench capacitor.

7. (Currently Amended) The integrated circuit according to claim [[5]] 1 wherein the capacitor is a quasi-static DRAM capacitor fabricated with nano-crystal oxide.

8. (Currently Amended) An integrated circuit comprising an array of DRAM cells, each DRAM cell comprising:

a first transistor having a gate coupled to a read word line and a drain coupled to a read bit line;

a second transistor coupled in series between the first transistor and a power supply voltage;

a third transistor coupled between the gate of the second transistor and a write bit line, a gate of the third transistor being coupled to a write word line; and

~~The integrated circuit according to claim 1 further comprising:~~

a CMOS inverter having an input coupled to the gate of the second transistor,

wherein the integrated circuit is a programmable integrated circuit, and an output of the CMOS inverter drives a pass gate that programmably couples interconnect lines on the programmable integrated circuit, and

wherein the write word line is not directly connected to the read word line.

9. (Original) The integrated circuit according to claim 8 wherein the third transistor is a p-channel field effect transistor, and the input of the CMOS inverter is not directly connected to an N-type doped semiconductor region.

10. (Original) The integrated circuit according to claim 1 further comprising:

a sense amplifier having an input coupled to the read bit line;

a multiplexer having a first input coupled to an output of the sense amplifier; and

a driver coupled between an output of the multiplexer and the write bit line.

11. (Original) The integrated circuit according to claim 10 further comprising:

a data shift register coupled to a second input of the multiplexer;

an error detection circuit coupled to an output of the data shift register, the error detection circuit performing error detection on data stored in the DRAM cells.

12. (Currently Amended) An integrated circuit comprising an array of DRAM cells, each DRAM cell comprising:

a first transistor having a gate coupled to a read word line and a drain coupled to a read bit line;

[[an]] a single inverter having an output coupled to a source of the first transistor; and

a second transistor coupled between an input of the single inverter and a write bit line, a gate of the second transistor being coupled to a write word line.

13. (Original) The integrated circuit as defined in claim 12 wherein the integrated circuit is a programmable integrated circuit and the output of the inverter is coupled to a pass gate.

14. (Original) The integrated circuit as defined in claim 12 wherein the second transistor is a p-channel transistor, and the input of the inverter is not directly connected to an N-type doped semiconductor region.

15. (Original) The integrated circuit as defined in claim 12 further comprising a capacitor coupled to the input of the inverter.

16. (Original) The integrated circuit as defined in claim 15 wherein the capacitor is a planar capacitor or a trench capacitor.

17. (Original) The integrated circuit as defined in claim 15 wherein the capacitor is a quasi-static DRAM capacitor fabricated with nano-crystal oxide.

18. (Original) The integrated circuit as defined in claim 12 further comprising:

a sense amplifier having an input coupled to the read bit line; and

a multiplexer coupled between an output of the sense amplifier and the write bit line.

19. (Currently Amended) A method for controlling programmable interconnects and logic functions ~~storing data in and accessing data~~ from a DRAM cell, the method comprising:

applying a first voltage on a write word line to turn on a first transistor;

applying a second voltage on a write bit line coupled to a drain of the first transistor to store charge at a gate of a second transistor, a capacitor being coupled to the gate of the second transistor to store a charge at the gate of the second transistor;

applying a third voltage on the write word line to turn off the first transistor; and

directly driving a gate voltage of a pass gate using the charge stored on the capacitor,

~~applying a fourth voltage on a read word line to turn on a third transistor, wherein the second transistor is coupled in series with third transistor; and~~

~~sensing a fifth voltage on a read bit line coupled to a drain of the third transistor, the second and third transistors conducting current between the read bit line and a supply voltage if the charge stored at the gate of the second transistor is a first logic state,~~

wherein the write word line is not directly connected to the read word line.

Claim 20. (Canceled)

21. (Currently Amended) The method according to claim 20, further comprising:

applying a fourth voltage on a read word line to turn on a third transistor, wherein the second transistor is coupled in series with third transistor; and

sensing a fifth voltage on a read bit line coupled to a drain of the third transistor, the second and third transistors conducting current between the read bit line and a supply voltage if the charge stored at the gate of the second transistor is a first logic state,

wherein a gate of a fifth pass gate transistor is coupled to the capacitor and the gate of the second transistor, the pass gate coupling two segments of programmable routing wires.

Claim 22. (Canceled)

23. (Currently Amended) The method according to claim [[22]] 19 wherein the first transistor is a p-channel transistor.

24. (Currently Amended) The method according to claim [[19]] 21 wherein sensing the fifth voltage on the read bit line further comprises:

amplifying the fifth voltage using a sense amplifier; and

driving an output signal of the sense amplifier to the write bit line to refresh the charge stored at gate of the second transistor.

25. (Currently Amended) The method according to claim [[19]] 21 further comprising:

detecting errors in the data stored in the DRAM cell.

26. (Currently Amended) A method for controlling programmable interconnects and logic functions ~~storing data in and accessing data~~ from a DRAM cell, the method comprising:

applying a first voltage on a write word line to turn on a first transistor;

applying a second voltage on a write bit line coupled to a drain of the first transistor to store charge at an input of an inverter;

applying a third voltage on the write word line to turn off the first transistor;

coupling the output of the inverter to a pass gate, the DRAM cell being part of a memory array of DRAM cells, the memory array and the pass gate being part of a programmable integrated circuit; and

directly driving a gate voltage of the pass gate using a charge stored on the capacitor.

~~applying a fourth voltage on a read word line to turn on a second transistor, wherein the second transistor is coupled to an output of the inverter; and~~

~~sensing a fifth voltage on a read bit line coupled to a drain of the second transistor, the second transistor conducting current between the read bit line and the output of the inverter if the charge stored at the input of the inverter is a first logic state.~~

27. (Original) The method according to claim 26 wherein the first transistor is a p-channel transistor and the second transistor is an n-channel transistor.

Claim 28. (Canceled)

29. (Currently Amended) The method according to claim 26 further comprising:

applying a fourth voltage on a read word line to turn on a second transistor, wherein the second transistor is coupled to an output of the inverter; and

sensing a fifth voltage on a read bit line coupled to a drain of the second transistor, the second transistor conducting current between the read bit line and the output of the inverter if the charge stored at the input of the inverter is a first logic state,

wherein sensing the fifth voltage on the read bit line further comprises:

amplifying the fifth voltage using a sense amplifier;

selecting an output signal of the sense amplifier using a multiplexer; and

driving an output signal of the multiplexer to the write bit line to refresh the charge stored at the input of the inverter.

30. (Original) The method according to claim 29 further comprising:

detecting errors in the data stored in the DRAM cell.

Claims 31-37. (Canceled)